WHAT IS CLAIMED IS:

1. A ferroelectric memory device, comprising:

a semiconductor substrate;

at least one interlayer dielectric layer on the semiconductor substrate;

an oxygen-diffusion barrier pattern having a plurality of sidewalls on the at least one interlayer dielectric layers;

an upper insulating layer on the at least one interlayer dielectric layer that at least partially surrounds the sidewalls of the oxygen-diffusion barrier pattern and that has a top surface that is higher than a top surface of the oxygen-diffusion barrier pattern; and

a capacitor, the capacitor having a bottom electrode that is on the oxygen-diffusion barrier pattern and overlaps at least a portion of the upper insulating layer, a ferroelectric layer on the bottom electrode, and a top electrode on the ferroelectric layer.

2. The ferroelectric memory device of Claim 1, wherein the oxygen-diffusion barrier pattern comprises at least one material selected from the group of iridium, ruthenium and osmium.

3. The ferroelectric memory device of Claim 2, wherein the oxygen-diffusion barrier pattern is formed of iridium and titanium aluminum nitride that are sequentially stacked or formed of iridium, titanium aluminum nitride and titanium that are sequentially stacked.

4. The ferroelectric memory device of Claim 1, wherein the bottom electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer.

5. The ferroelectric memory device of Claim 4, wherein the top electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer.

6. The ferroelectric memory device of Claim 1, further comprising:

a transistor having a gate electrode formed on the semiconductor substrate and source/drain regions at both sides of the gate electrode; and

a conductive contact plug that penetrates one or more of the at least one interlayer dielectric layers to electrically connect one of the source/drain regions and the oxygen-diffusion barrier pattern.

7. The ferroelectric memory device of Claim 1, further comprising:

a first insulating layer on the upper insulating layer that surrounds sidewalls of the capacitor;

a lower interconnection on the upper insulating layer and on the top electrode;

second and third insulating layers sequentially stacked on the lower interconnection and the first insulating layer; and

an upper interconnection penetrating the third and second insulating layers to electrically connect to the lower interconnection.

8. The ferroelectric memory device of Claim 1, wherein the surface area of a top surface of the bottom electrode exceeds the surface area of a top surface of the oxygen-diffusion barrier pattern, and wherein the bottom electrode shields the ferroelectric layer from contact with the oxygen-diffusion barrier pattern.

9. A ferroelectric memory device, comprising:

a semiconductor substrate;

a lower insulating layer on the semiconductor substrate;

a plug penetrating the lower insulating layer, the plug being electrically connected to the semiconductor substrate;

an upper insulating layer on the lower insulating layer, the upper insulating layer having an opening to expose the plug and a portion of the lower insulating layer;

an oxygen-diffusion barrier pattern in the opening, wherein a top surface of the oxygen-diffusion barrier pattern is lower than a top surface of the upper insulating layer; and

a capacitor that is electrically connected to the plug, the capacitor having a bottom electrode that is on the oxygen-diffusion barrier pattern and on at least a portion of the upper insulating layer, a ferroelectric layer on the bottom electrode, and a top electrode on the ferroelectric layer.

10. The ferroelectric memory device of Claim 9, wherein the oxygen-diffusion barrier pattern comprises at least one material selected from the group of iridium, ruthenium and osmium.

11. The ferroelectric memory device of Claim 9, wherein the bottom electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer, and wherein the top electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer.

12. The ferroelectric memory device of Claim 9, wherein the surface area of a top surface of the bottom electrode exceeds the surface area of a top surface of the oxygen-diffusion barrier pattern, and wherein the bottom electrode shields the ferroelectric layer from contact with the oxygen-diffusion barrier pattern.

13. A method of fabricating a ferroelectric memory device, the method comprising:

forming a lower insulating layer including a conductive plug on a semiconductor substrate;

forming an oxygen-diffusion barrier pattern that is electrically connected to the conductive plug and forming an upper insulating pattern on the lower insulating layer, wherein the upper insulating pattern and the oxygen-diffusion barrier pattern are formed such that the upper insulating pattern surrounds sidewalls of the oxygen-diffusion barrier pattern and a top surface of the upper insulating pattern is higher than a top surface of the oxygen-diffusion barrier pattern;

forming a lower electrode layer on the upper insulating pattern and the oxygen-diffusion barrier pattern;

forming a ferroelectric layer on the lower electrode layer; and

forming an upper electrode layer on the ferroelectric layer.

14. The method of Claim 13, wherein the forming the oxygen-diffusion barrier pattern comprises:

forming a conductive oxygen-diffusion barrier layer and a hard mask layer on the lower insulating layer; and

patterning the hard mask layer and the conductive oxygen-diffusion barrier layer to be electrically connected to the contact plug.

15. The method of Claim 14, wherein forming the upper insulating pattern comprises:

forming an upper insulating layer on the lower insulating layer, the oxygen-diffusion barrier pattern and the hard mask pattern;

planarizingly etching the upper insulating layer using the hard mask pattern as a planarization stop to form the upper insulating pattern; and

selectively removing the hard mask pattern.

16. The method of Claim 15, wherein the hard mask layer is formed of a material having etch selectivity with respect to the upper insulating layer.

17. The method of Claim 15, wherein the hard mask layer is formed of a material including nitrogen.

18. The method of Claim 17, wherein the material including nitrogen comprises titanium nitride, silicon nitride or titanium aluminum nitride.

19. The method of Claim 13, wherein forming the upper insulating pattern comprises:

forming an upper insulating layer on the lower insulating layer; and

patterning the upper insulating layer to form the upper insulating pattern and to form an opening exposing the conductive plug.

20. The method of Claim 19, wherein forming the oxygen-diffusion barrier pattern comprises:

forming an oxygen-diffusion barrier layer in the opening; and

etching a portion of the oxygen-diffusion barrier layer filling the opening.

21. The method of Claim 13, wherein the oxygen-diffusion barrier pattern is a single layer pattern formed of iridium, ruthenium or osmium, a double layer pattern formed of sequentially stacked iridium and titanium aluminum nitride or a

triple layer pattern formed of sequentially stacked iridium, titanium aluminum nitride and titanium.

22. The method of Claim 13, wherein the upper electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer, and wherein the lower electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer.

23. The method of Claim 22, wherein the noble metal oxide electrode includes iridium oxide, ruthenium oxide, lanthanum strontium cobalt oxide (LSCO), yttrium barium cobalt oxide (YBCO) or lanthanum nickel oxide (LNO).

24. The method of Claim 22, wherein the noble metal comprises platinum, iridium, ruthenium, osmium, and lanthanum.

25. The method of Claim 13, wherein forming the ferroelectric layer comprises depositing the ferroelectric layer on the entire surface of the lower electrode layer.

26. A method of forming a ferroelectric memory device comprising:

forming a lower insulating layer including a contact plug on a semiconductor substrate;

forming an upper insulating layer on the lower insulting layer;

patterning the upper insulating layer to form an opening exposing the conductive plug and the lower insulating layer;

forming an oxygen-diffusion barrier pattern in the opening such that a top surface of the oxygen-diffusion barrier pattern is lower than a top surface of the upper insulating layer;

forming a lower electrode layer on the upper insulating layer and on the oxygen-diffusion barrier pattern;

forming a ferroelectric layer on the lower electrode layer

forming an upper electrode layer on the ferroelectric layer; and

patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer.

27. The method of Claim 26, wherein the oxygen-diffusion barrier pattern is a single layer pattern formed of iridium, ruthenium or osmium, a double layer pattern formed of sequentially stacked iridium and titanium aluminum nitride or a triple layer pattern formed of sequentially stacked iridium, titanium aluminum nitride and titanium.

28. The method of Claim 26, wherein the lower electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer, and wherein the upper electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer.